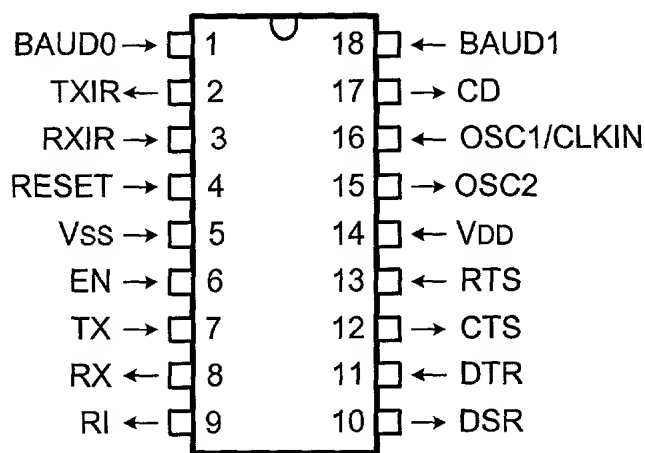


CLAIMS

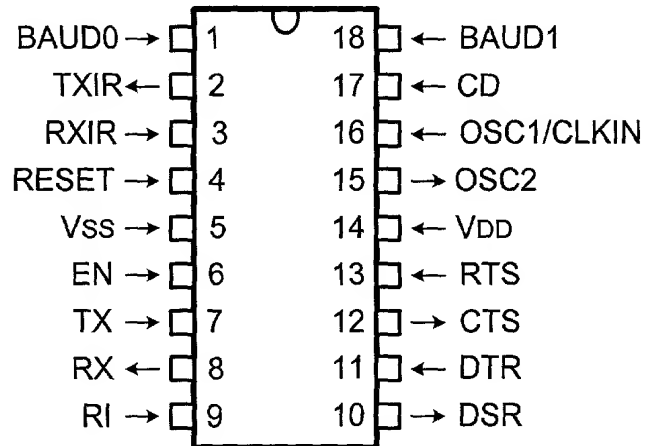
What is claimed is:

1. An integrated circuit (IC) functional pathway configuration of connections, comprising: BAUD0, TXIR, RXIR, RESET, VSS, EN, TX, RX, RI, DSR, DTR, CTS, RTS, VDD, OSC2, OSC1/CLKIN, CD and BAUD1.

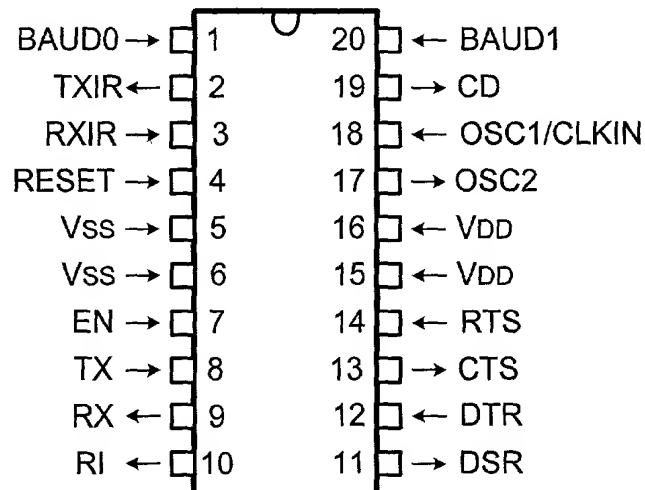
2. The IC functional pathway configuration according to claim 1, wherein the connections are arranged as follows:



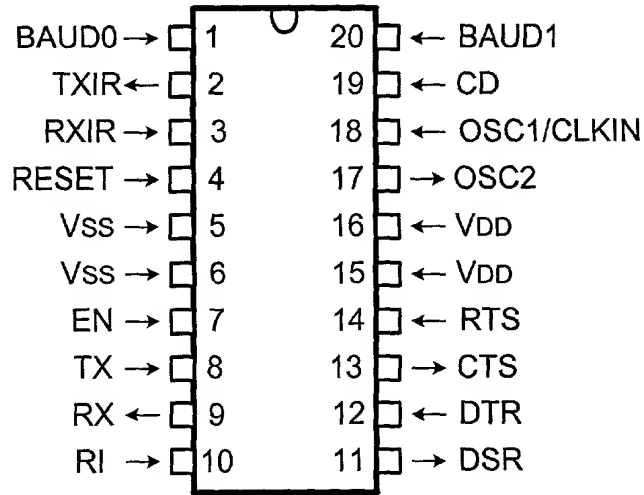
- 1            3.        The IC functional pathway configuration according to claim 1, wherein the  
2        connections are arranged as follows:



- 1            4.        The IC functional pathway configuration according to claim 1, wherein the  
2        connections are arranged as follows:



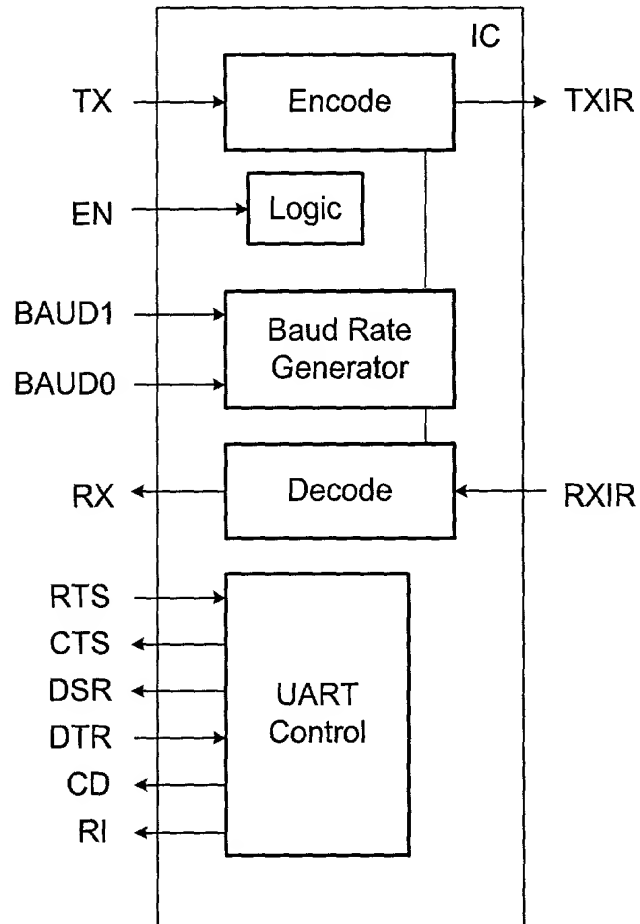
- 3           5.       The IC functional pathway configuration according to claim 1, wherein the  
4       connections are arranged as follows:



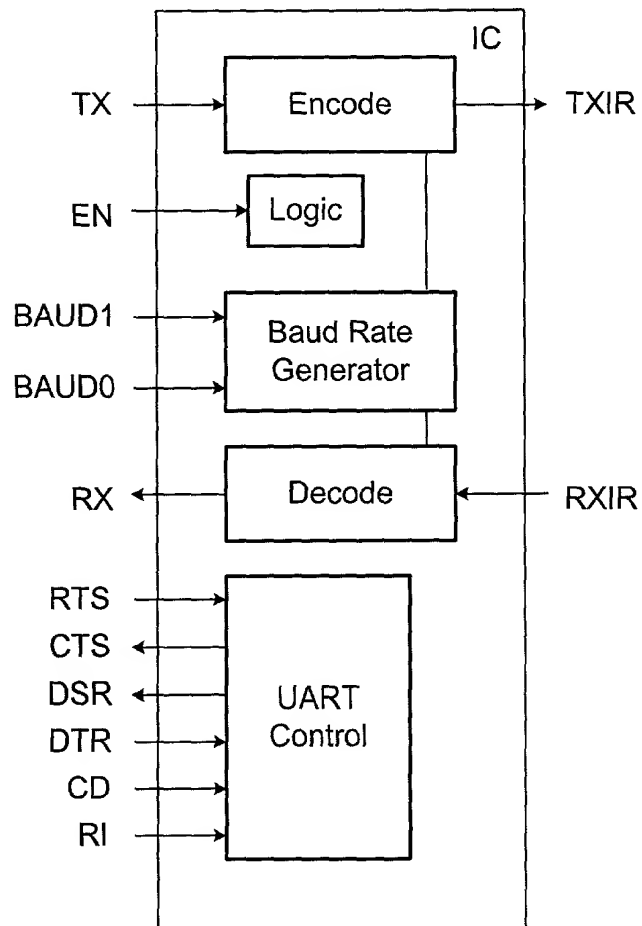
- 5           6.       A functional pathway configuration for an encode/decode function,  
6       comprising:  
7           an encode TX function input and an encode TXIR function output;  
8           a decode RXIR function input and a decode RX function output;  
9           a logic EN function input;  
10          a logic RESET function input;  
11          at least one logic BAUD function input; and  
12          UART function inputs and outputs.

- 1           7.       The functional pathway configuration according to claim 6, wherein the  
2       UART function inputs and outputs are selected from the group consisting of RTS, CTS,  
3       DSR, DTR, CD and RI.

- 1           8.       A functional pathway configuration for an integrated circuit (IC) including  
2       encode/decode functions, logic, baud rate generator and UART control as follows:



- 1            9.        A functional pathway configuration for an integrated circuit (IC) including
- 2        encode/decode functions, logic, baud rate generator and UART control as follows:



- 1           10.    The functional pathway configuration according to claims 8 or 9, wherein  
2    pathway configuration function connections are arranged as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	EN
P7	TX
P8	RX
P9	RI
P10	DSR
P11	DTR
P12	CTS
P13	RTS
P14	VDD
P15	OSC2
P16	OSC1/CLKIN
P17	CD
P18	BAUD1

- 1            11.    The functional pathway configuration according to claims 8 or 9, wherein
- 2    pathway configuration function connections are arranged as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	VSS
P7	EN
P8	TX
P9	RX
P10	RI
P11	DSR
P12	DTR
P13	CTS
P14	RTS
P15	VDD
P16	VDD
P17	OSC2
P18	OSC1/CLKIN
P19	CD
P20	BAUD1

- 1           12.    A functional pathway configuration for an encoder/decoder, comprising:  
2                   a first set of nine connections P1, P2 . . . P9, wherein each of the first set of  
3           nine connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	EN
P7	TX
P8	RX
P9	RI

4           and;



5 a second set of nine connections P10, P9 . . . P18, wherein each of the  
6 second set of nine connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P10	DSR
P11	DTR
P12	CTS
P13	RTS
P14	VDD
P15	OSC2
P16	OSC1/CLKIN
P17	CD
P18	BAUD1

7 wherein at least one of the sets is disposed on one side of an integrated  
8 circuit package.

- 1           13.    A functional pathway configuration for an encoder/decoder, comprising:  
2                   a first set of ten connections P1, P2 . . . P10, wherein each of the first set of  
3           ten connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	VSS
P7	EN
P8	TX
P9	RX
P10	RI

4                   and;

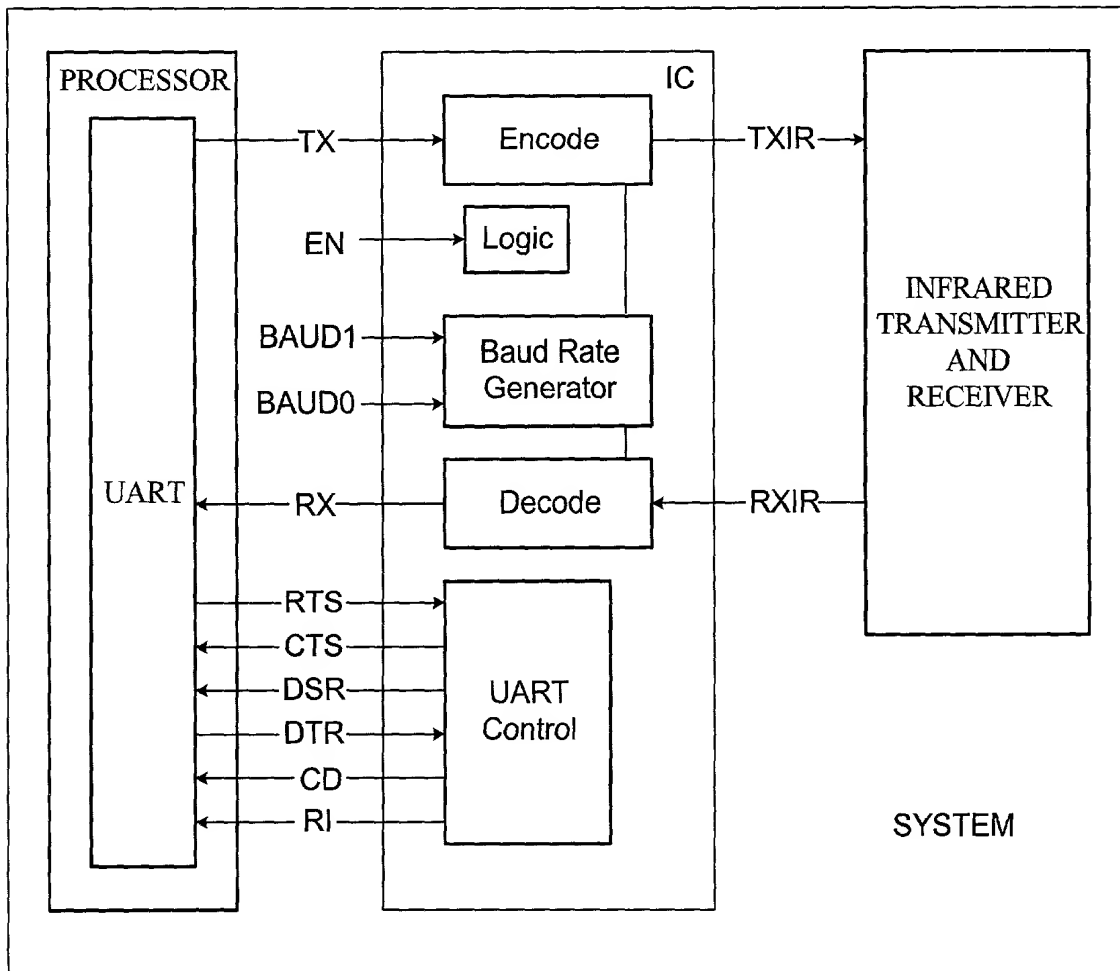
5 a second set of ten connections P11, P9 . . . P20, wherein each of the second  
 6 set of ten connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P11	DSR
P12	DTR
P13	CTS
P14	RTS
P15	VDD
P16	VDD
P17	OSC2
P18	OSC1/CLKIN
P19	CD
P20	BAUD1

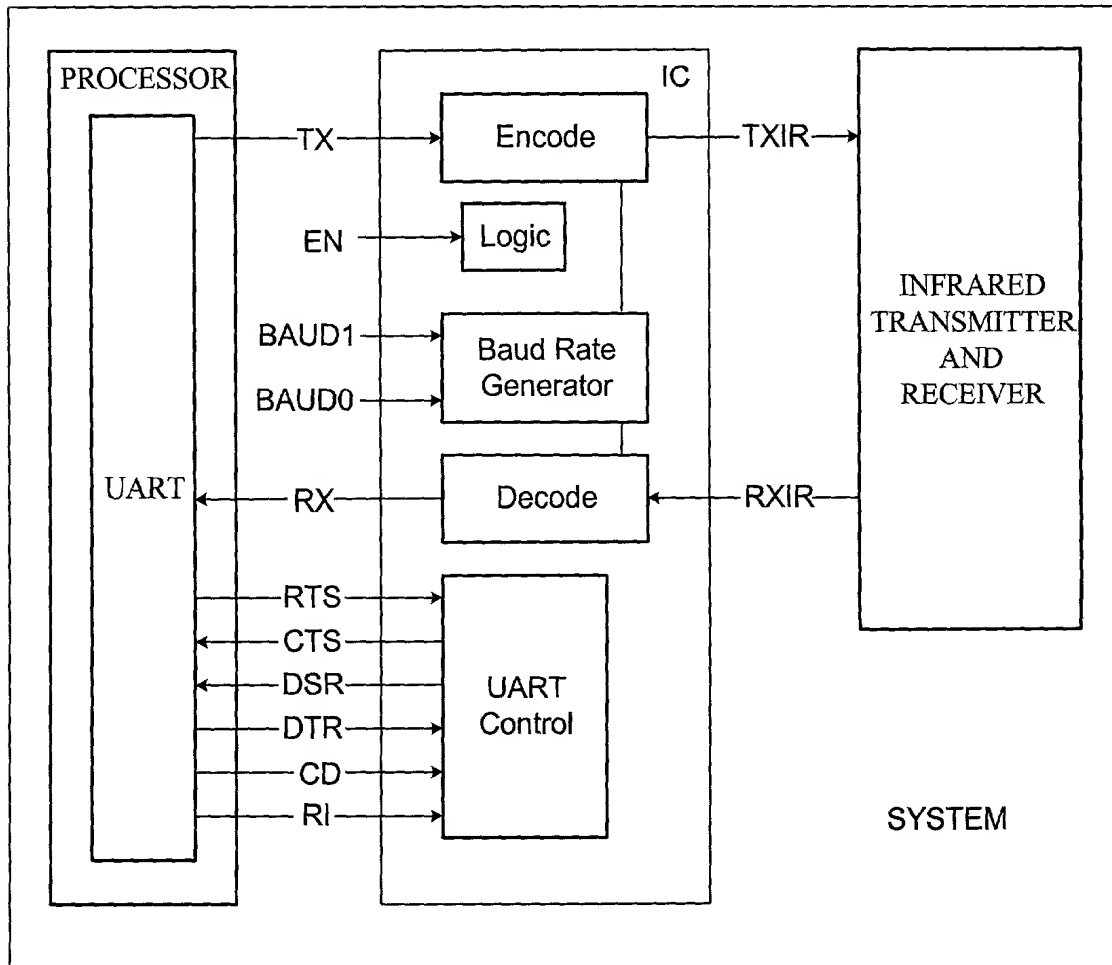
7 wherein at least one of the sets is disposed on one side of an integrated  
 8 circuit package.

1 14. A system having a functional pathway configuration for an interface  
 2 between an integrated circuit (IC) and a system in which the IC is embedded, comprising:  
 3 BAUD0, TXIR, RXIR, RESET, VSS, EN, TX, RX, RI, DSR, DTR, CTS, RTS, VDD,  
 4 OSC2, OSC1/CLKIN, CD and BAUD1.

- 1           15.    A functional pathway configuration for an interface between a system  
2   including a UART, an infrared transmitter and receiver, and an integrated circuit (IC)  
3   embedded in the system, comprising:



- 1           16. A functional pathway configuration for an interface between a system  
 2 including a UART, an infrared transmitter and receiver, and an integrated circuit (IC)  
 3 embedded in the system, comprising:



- 1           17.    The functional pathway configuration according to claims 15 or 16, wherein:
- 2                   a UART output interfaces with a function TX;
- 3                   the UART input interfaces with a function RX;
- 4                   an infrared transmitter input interfaces with a function TXIR; and
- 5                   an infrared receiver output interfaces with a function RXIR.

- 1           18.     The functional pathway configuration according to claims 15 or 16, wherein  
2     pathway configuration function connections are arranged as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	EN
P7	TX
P8	RX
P9	RI
P10	DSR
P11	DTR
P12	CTS
P13	RTS
P14	VDD
P15	OSC2
P16	OSC1/CLKIN
P17	CD
P18	BAUD1

- 1            19.    The functional pathway configuration according to claims 15 or 16, wherein
- 2    pathway configuration function connections are arranged as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	VSS
P7	EN
P8	TX
P9	RX
P10	RI
P11	DSR
P12	DTR
P13	CTS
P14	RTS
P15	VDD
P16	VDD
P17	OSC2
P18	OSC1/CLKIN
P19	CD
P20	BAUD1



1           20.    The functional pathway configuration according to claims 15 or 16, further  
2 comprising:

3                   a first set of nine connections P1, P2 . . . P9, wherein each of the first set of  
4           nine connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	EN
P7	TX
P8	RX
P9	RI

5           and;

6 a second set of nine connections P10, P9 . . . P18, wherein each of the  
7 second set of nine connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P10	DSR
P11	DTR
P12	CTS
P13	RTS
P14	VDD
P15	OSC2
P16	OSC1/CLKIN
P17	CD
P18	BAUD1

8 wherein at least one of the sets is disposed on one side of an integrated  
9 circuit package.

1           21.     The functional pathway configuration according to claims 15 or 16, further  
2 comprising:

3                   a first set of ten connections P1, P2 . . . P10, wherein each of the first set of  
4 ten connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P1	BAUD0
P2	TXIR
P3	RXIR
P4	RESET
P5	VSS
P6	VSS
P7	EN
P8	TX
P9	RX
P10	RI

5                   and;

6 a second set of ten connections P11, P9 . . . P20, wherein each of the second  
7 set of ten connections has a dedicated function(s) as follows:

CONNECTION	FUNCTION(S)
P11	DSR
P12	DTR
P13	CTS
P14	RTS
P15	VDD
P16	VDD
P17	OSC2
P18	OSC1/CLKIN
P19	CD
P20	BAUD1

8 wherein at least one of the sets is disposed on one side of an integrated  
9 circuit package.

1 22. The functional pathway configuration according to claim 15, wherein the  
2 system is data terminal equipment (DTE).

1 23. The functional pathway configuration according to claim 16, wherein the  
2 system is data communication equipment (DCE).